



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,156	07/14/2006	Yasuyuki Arai	0756-7774	5647
31780	7590	10/29/2009		
ERIC ROBINSON PMB 955 21010 SOUTHBANK ST. POTOMAC FALLS, VA 20165			EXAMINER TAYLOR, APRIL ALICIA	
			ART UNIT	PAPER NUMBER
			2887	
			MAIL DATE	DELIVERY MODE
			10/29/2009	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/586,156

**Applicant(s)**

ARAI ET AL.

**Examiner**

APRIL A. TAYLOR

**Art Unit**

2887

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 June 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3,6-10 and 13-36 is/are rejected.
- 7) ☒ Claim(s) 4,5,11 and 12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SI/08)  
Paper No(s)/Mail Date 6/25/09
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

Receipt is acknowledged of the Amendment filed June 25, 2009. Claims 1-36 are pending in the application.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 6-10, and 13-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kano et al (US 6,522,549) (hereinafter Kano) in view of Reddy (US 20020094639 A1).

Re claims 1, 2, 8 and 9: Kano teaches an IC card (1) including:

a label substratum (2) over which an antenna is formed;  
an integrated circuit device (7) provided in contact with the label substratum;  
a separating sheet (3a, 3b); and  
an adhesive provided between the label substratum and the separating sheet;  
and

wherein the antenna and the integrated circuit device are connected through a cross wiring. (See col. 4, line 25 to col. 5, line 13)

Kano fails to specifically teach or fairly suggest wherein the integrated circuit device includes a thin film transistor.

Reddy discloses a RFID tag having an integrated circuit device including a thin film transistor (see paragraphs 0027-0029). In view of Reddy's teaching, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to employ the well known thin film transistor to the teachings of Kano in order to reduce the cost of the IC card.

Re claims 3, and 10: Kano teaches wherein a protective layer (4a, 4b) comprising a single layer or stacked layers containing silicon oxide, silicon nitride or silicon oxynitride is formed on at least one of an upper surface and a lower surface of the integrated circuit device (see col. 5, lines 14+).

Re claims 6 and 13: Kano teaches wherein a size of the integrated circuit device is 0.09 to 25 mm<sup>2</sup> (see col. 4, lines 55+).

Re claims 7 and 14: Kano teaches wherein a thickness of the integrated circuit device is 0.1 to 3  $\mu$ m (see col. 4, lines 55+).

Re claims 15-17, 19-21, 23-25, 27-29, 31 and 33: Kano teaches an IC card including:

- a card substratum over which an antenna is formed;
- an integrated circuit device provided in contact with card substratum;
- a cover for covering at least a side of the card substratum where an antenna and the integrated circuit device are formed;

wherein the antenna and the integrated circuit device are connected through a cross wiring;

wherein the cover comprises resin and is formed by a laminating method.

Kano fails to specifically teach or fairly suggest wherein the integrated circuit device includes a thin film transistor.

Reddy discloses a RFID tag having an integrated circuit device including a thin film transistor (see paragraphs 0027-0029). In view of Reddy's teaching, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to employ the well known thin film transistor to the teachings of Kano in order to reduce the cost of the IC card.

Re claims 18, 22, 26, 30, 32, and 34: Kano teaches wherein a protective layer comprising a single layer or stacked layers containing silicon oxide, silicon nitride or silicon oxynitride is formed on at least one of the upper surface and the lower surface of the integrated circuit device.

Re claim 35: Kano teaches IC card including:

a label substratum having a first surface and a second surface opposing to the first surface;

an antenna formed over the first surface of the label substratum;

an integrated circuit device over the first surface of the label substratum;

a wiring formed on the second surface of the label substratum;

a separating sheet provided over the first surface of the label substratum with an adhesive layer, antenna, and the integrated circuit device interposed therebetween,

wherein the wiring electrically connects the integrated circuit device and a part of the antenna through a contact hole formed in the label substratum. (See col. 4, line 25 to col. 5, line 26)

Kano fails to specifically teach or fairly suggest wherein the integrated circuit device includes a thin film transistor.

Reddy discloses a RFID tag having an integrated circuit device including a thin film transistor (see paragraphs 0027-0029). In view of Reddy's teaching, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to employ the well known thin film transistor to the teachings of Kano in order to reduce the cost of the IC card.

Re claim 36: Kano teaches IC card including:

a label substratum; an antenna formed over the label substratum; an insulating layer over the antenna; a wiring formed on the insulating layer; an integrated circuit device over the label substratum; a separating sheet provided over the label substratum with an adhesive layer, the antenna, and insulating layer, and the integrated circuit

device interposed therebetween, wherein the wiring is connected to the antenna through a contact hole formed in the insulating layer. (See col. 4, line 25 to col. 5, line 26)

Kano fails to specifically teach or fairly suggest wherein the integrated circuit device includes a thin film transistor.

Reddy discloses a RFID tag having an integrated circuit device including a thin film transistor (see paragraphs 0027-0029). In view of Reddy's teaching, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to employ the well known thin film transistor to the teachings of Kano in order to reduce the cost of the IC card.

#### ***Allowable Subject Matter***

Claims 4, 5, 11, and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Re claims 4 and 11: The prior of record, taken alone or in combination, fail to teach or fairly suggest, in conjunction with other limitations in the claims, wherein in the case where the protective layer is formed on the upper surface and the lower surface of the thin film integrated circuit device, it is placed the thin film integrated circuit device at

a position of (d/2)  $\pm$  30  $\mu$ m or less when a total thickness of the thin film integrated circuit device and the top and bottom protective films is d.

Re claims 5 and 12: The prior of record, taken alone or in combination, fail to teach or fairly suggest, in conjunction with other limitations in the claims, wherein a semiconductor film of the thin film transistor included in the thin film integrated circuit device contains hydrogen or halogen of 0.0005 to 5 atomic %.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Inoue et al (US 6,700,631); Reddy (US 6,509,217); Atherton (US 6,888,509); and Morizumi et al (US 6,459,588)

### ***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to APRIL A. TAYLOR whose telephone number is (571)272-2403. The examiner can normally be reached on Monday - Friday from 7:00AM - 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven S. Paik can be reached on (571) 272-2404. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thien M. Le/  
Primary Examiner, Art Unit 2887

/AAT/  
Examiner, AU 2887  
October 26, 2009